The Next Digisonde

Theme: Fully Software Based (almost)

Moving away from custom ASICs

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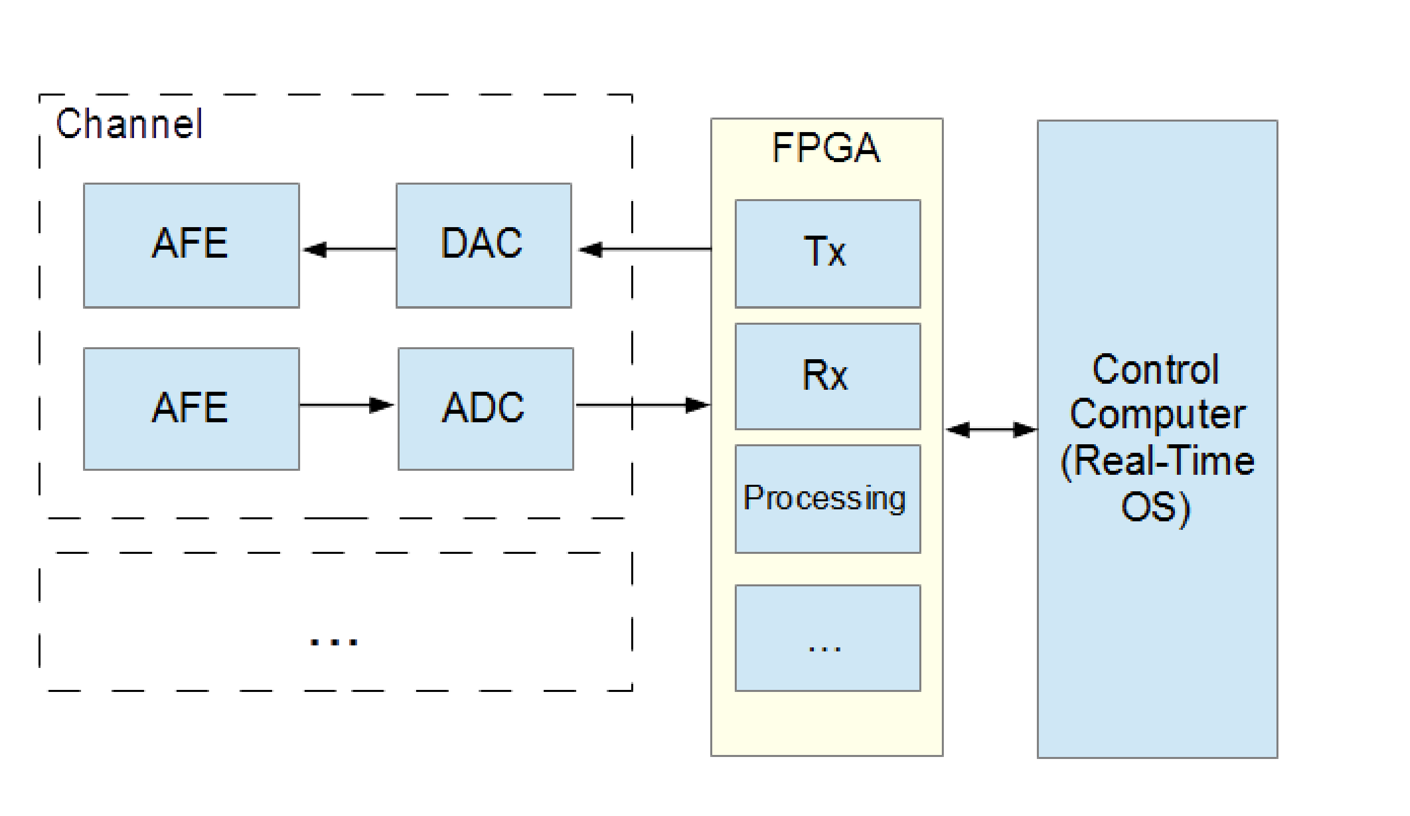
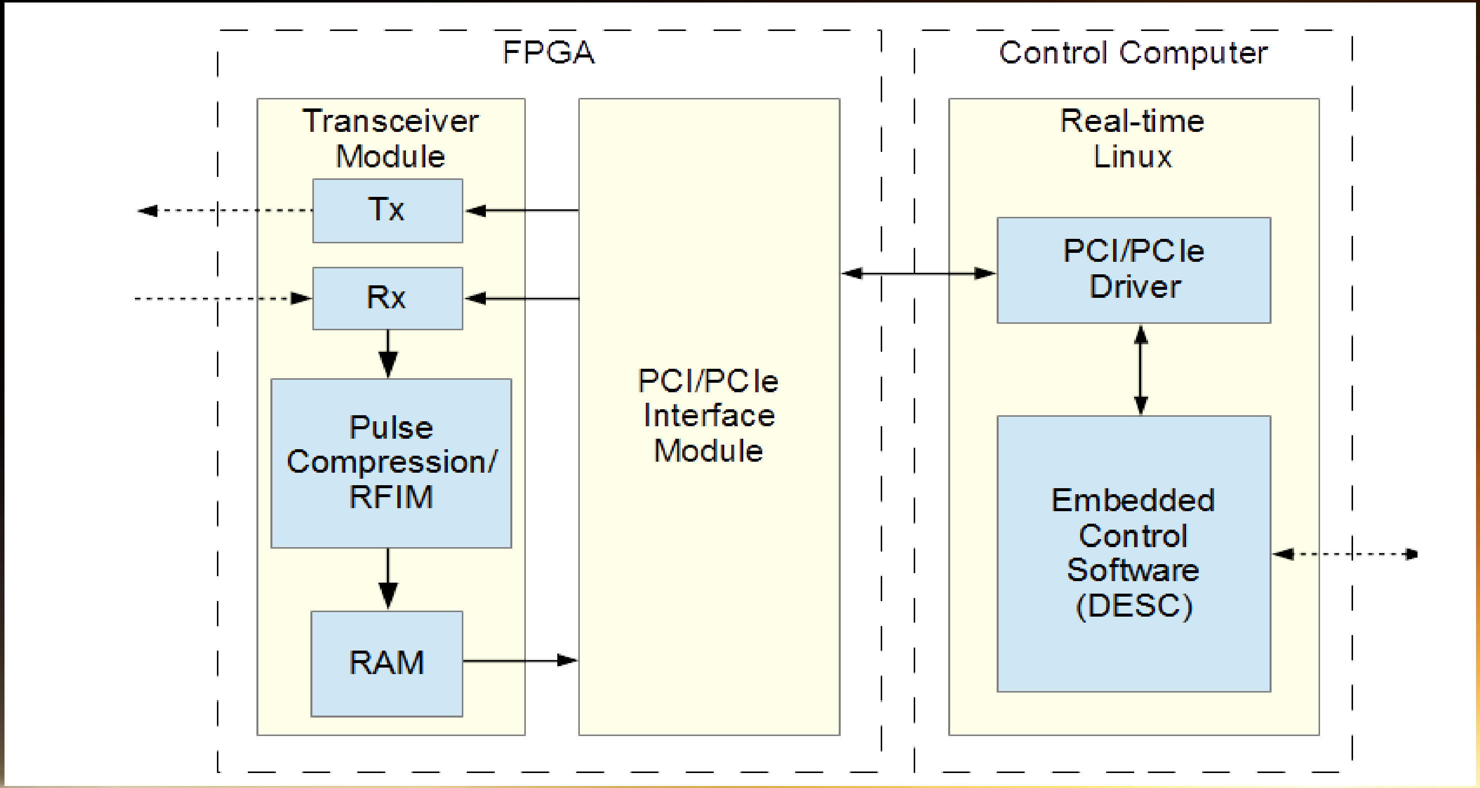
Problems with current approach

- Uses a number of Application Specific ICs
  - These become obsolete over time
  - Requires system to be re-engineered using newer parts
- Complex board-level design
- New features often require hardware changes

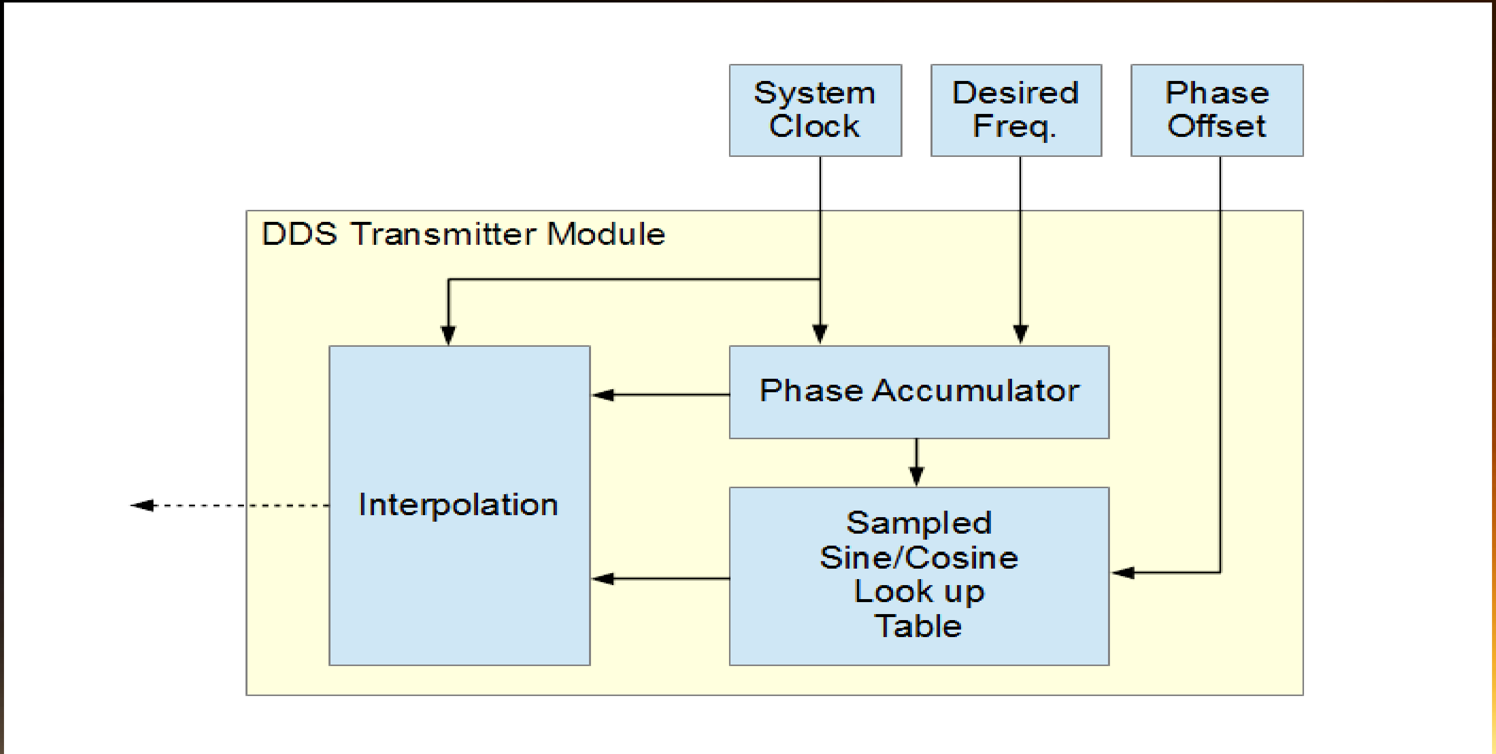
Hardware Architecture



Single Channel Architecture



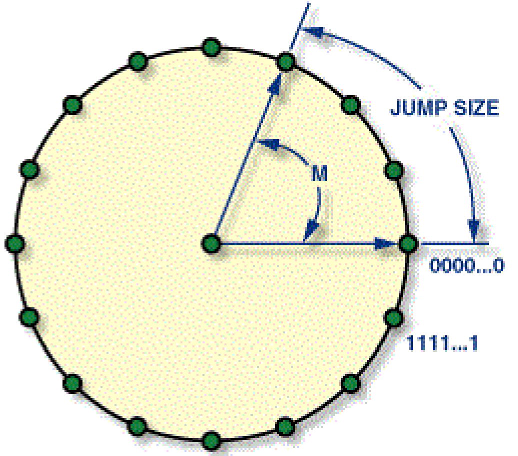
Direct Digital Synthesis Transmitter



Understanding Direct Digital Synthesis

$$f_{out} = \frac{M \cdot f_c}{2^n}$$

- Where:
  - fout = synthesized output frequency
  - M = digital tuning “step” value
  - fc = digital reference clock
  - n = width of phase accumulator in bits

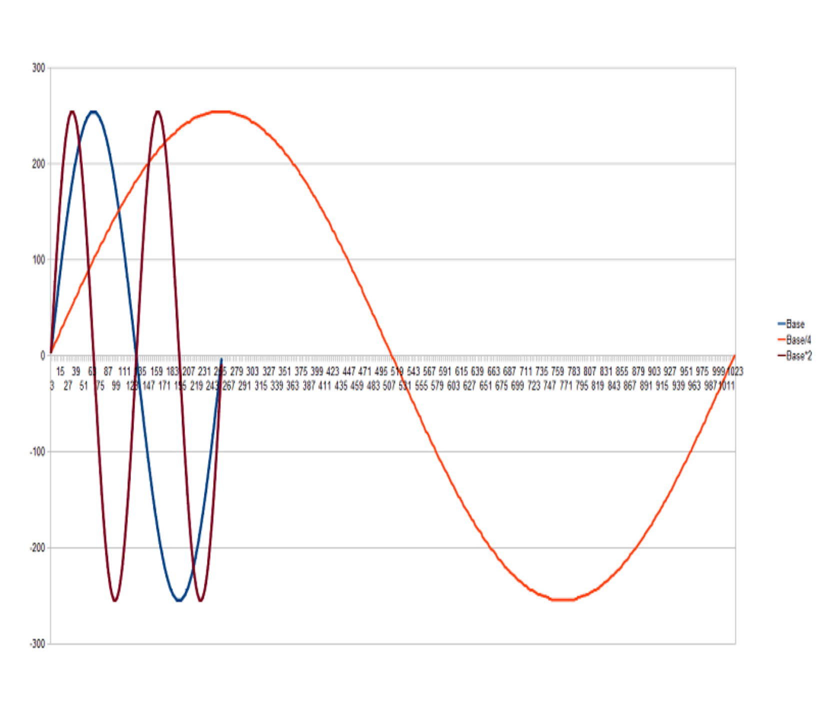


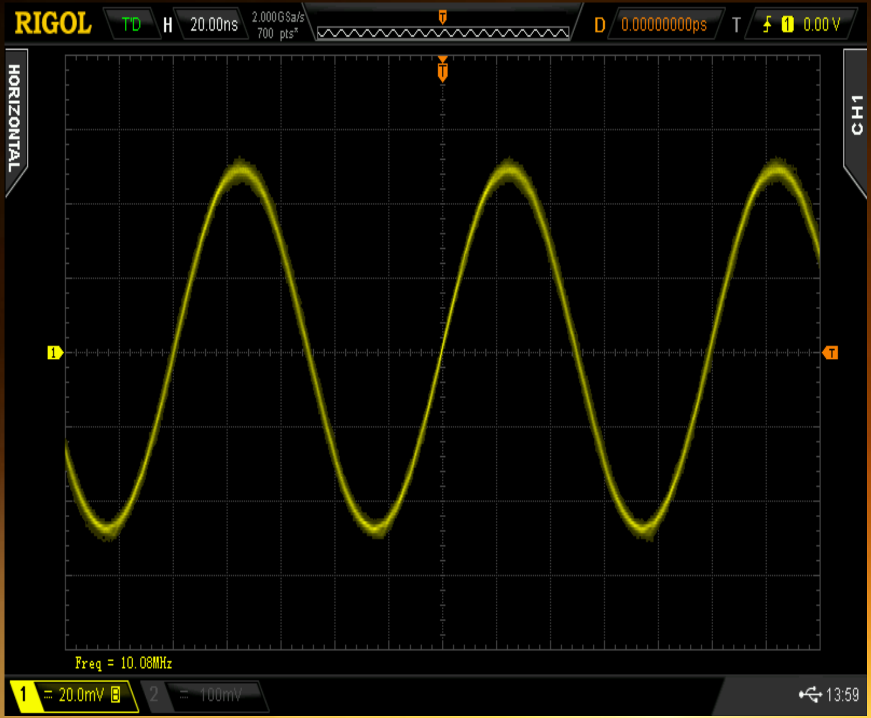
n	NUMBER OF POINTS
8	256
12	4096
16	65535
20	1048576
24	16777216
28	268435456
32	4294967296
48	281474976710656

DDS Advantages (implemented in FPGA)

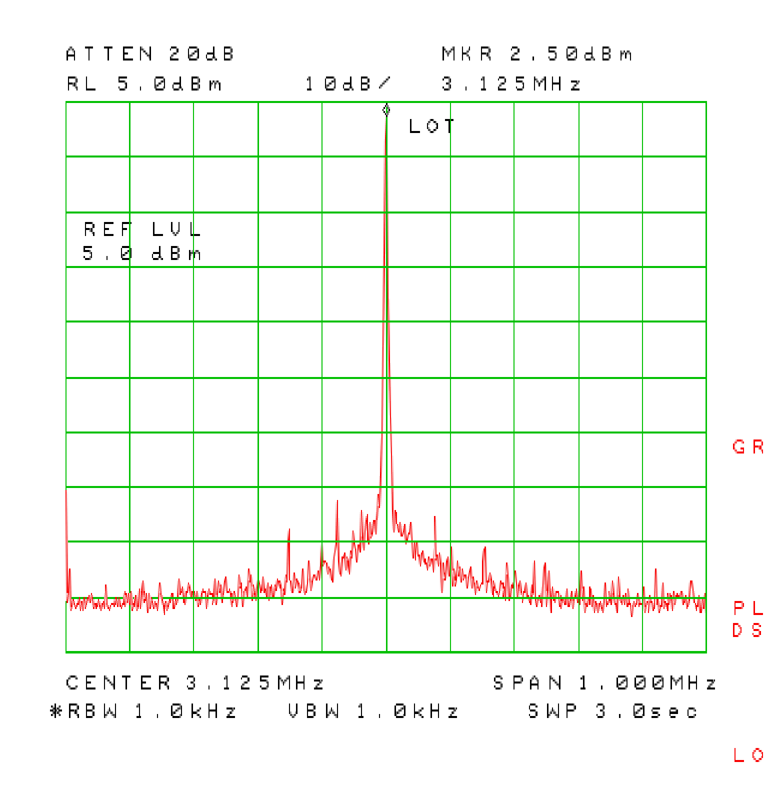
- Frequency resolution of fc/2^n !
- Extremely flexible / reconfigurable
  - Field updates for improved performance
- No longer tied to specific hardware ASICs

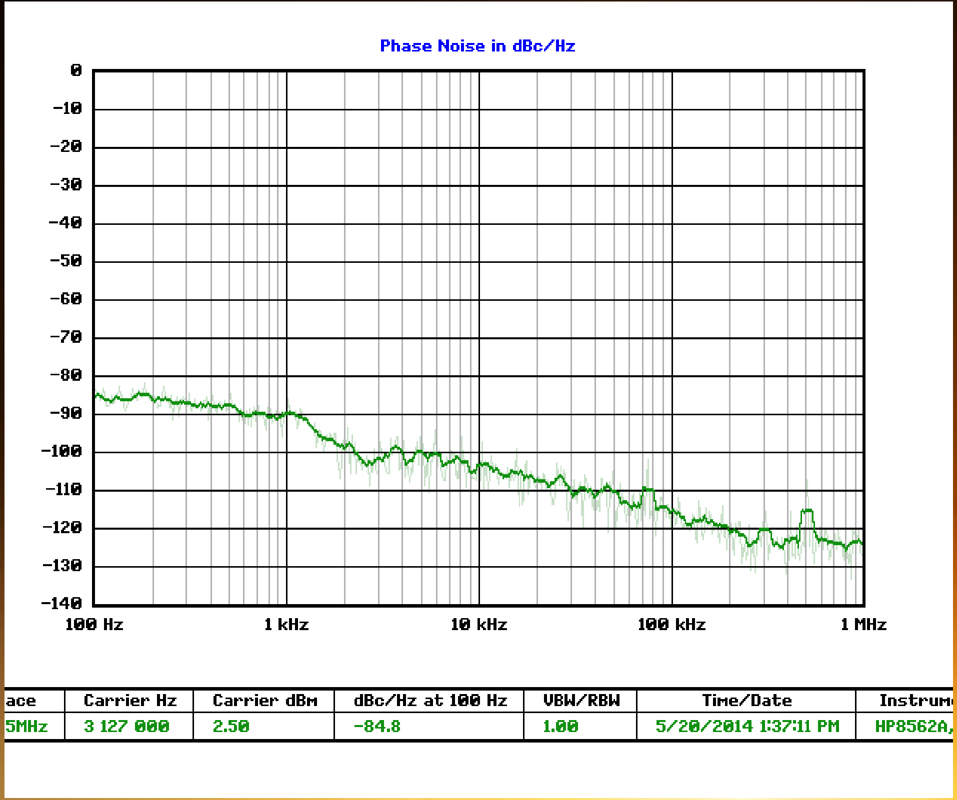
Sampled Waveform, Reconstructed



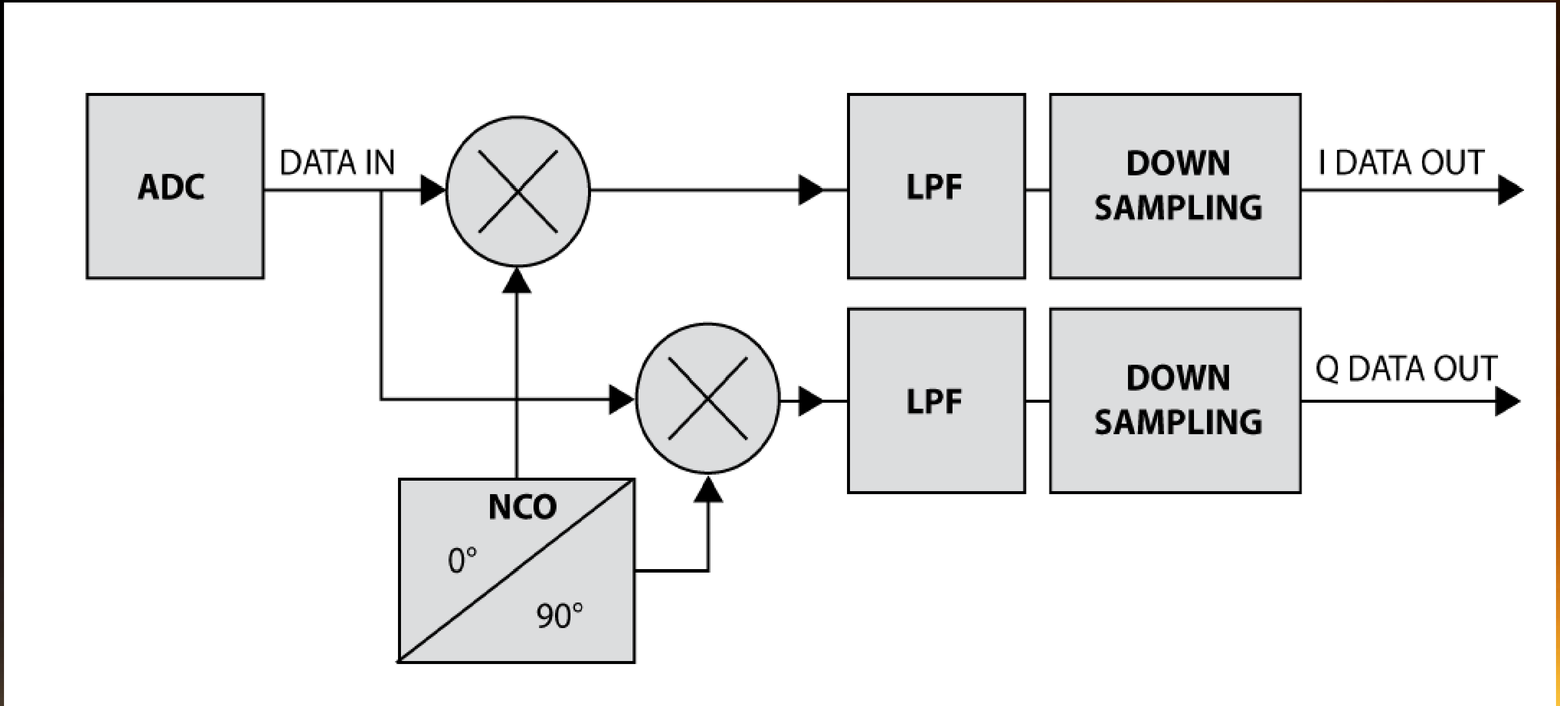


Synthesized Waveform, Frequency Domain





Receiver Details

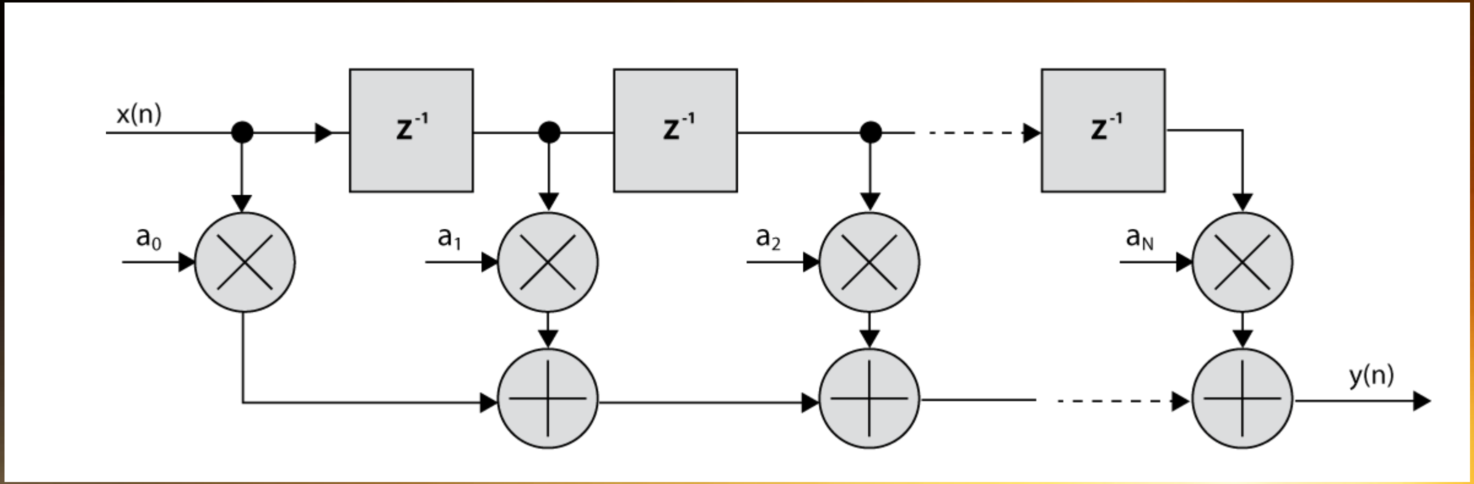


Receiver Details

- Real samples mixed with complex LO
  - All following stages done in complex domain
- Digital down conversion process
  - Finite Impulse Response (FIR) Filter (21-tap)
  - Re-sampling at ~60 kHz (pulse bandwidth = 30 kHz)

- FIR low-pass filter
  - Easily implemented in FPGA
  - Response easily adjusted by adding/removing stages

$$y(n) = \sum_{i=0}^{N-1} a_i x(n-i)$$



- Post Processing
  - Discrete Fourier Transform
  - Radio Frequency Interference Mitigation
    - Determine interference frequency w/ greatest magnitude
    - Synthesize out-of-phase signal
    - Iterative process

Dalu

감사합니다

Gracias Danke Ευχαριστίες

Obrigado

THANK YOU

Köszönöm

Спасибо Dank

Grazie

ありがとう

Tack 谢谢 Merci

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