Digisonde 4D Overview

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Digisonde 4D





Outline

- Digisonde System Introduction
- Transceiver Hardware Overview
- Current Work and Future Digisonde Development



Key 4D Innovations

Digital Transceiver

- Superior accuracy, precision, and resolution of amplitude and phase measurements
 - Precision Echolocation for skymaps
 - Improved lonogram fidelity
- Simpler to build and maintain
- Embedded platforms
 - Faster processors and interfaces
 - Fast enough to record time domain raw data
 - No more pauses within a measurement



Key 4D Innovations (2)

- New Signal Processing
 - RFI Mitigation technique (~30 dB SNR improvement)
 - Faster measurements (2 sec ionograms)
- Software and Data Analysis
 - New DCART terminal for real-time data monitoring and processing, experiment planning and system commanding
 - New passive mode for reception of signals from transmitters-of-opportunity
 - Fault isolation to LRM with instructions to the engineer
- Exact Reproducible Timing
 - Automatic bi-static sounding



Improved Ionogram Fidelity



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Precision Echolocation



Echolocation with 4D at Trivandrum, India

Real ionosphere, not a lab shelf calibration





Rapid Ionograms

🕌 Survey



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Simplified Architecture





Embedded Systems



DPS-4D Digital Transceiver Block Diagram



Digisonde 4D General Layout



Development of Topside Sounder

- Much of the Digisonde 4D digital transceiver technology is applicable to a topside sounder
- Current transceiver hardware is unacceptable for space
- Implement a digital transceiver that is suitable for space (in FPGA)
- Use the development knowledge and apply it to the ground system



Field Programmable Gate Array (FPGA)

- An integrated circuit designed to be configured by a customer or a designer after manufacturing hence "field programmable"
- Contemporary FPGAs have large resources of logic gates and RAM blocks to implement complex digital designs
- The FPGA configuration is specified using a hardware description language (HDL) code
- FPGAs can be used to implement any logical function that an ASIC could perform
- The ability to update the functionality after shipping, partial reconfiguration of a portion of the design and the low non-recurring engineering offer advantages for many applications



Future Direction of Digisonde

- Implement transceiver in Field Programmable Gate Array (FPGA)
 - Consolidation of components (Transmitter / Receiver / Pre-Processor / BIT)
 - Functionality is implemented as firmware (code) and is more portable
 - Greater control over functionality
 - The resulting IP can be applied to different devices to suit various applications (space, for example)
- Replace RTEMS (Real Time Executive for Multiprocessor Systems) with Real Time Linux
 - Better Hardware support allows more flexibility in choosing future computers
 - Large support community
- Selected PCI as transceiver / computer interface (instead of IDE and LPT)
 - More than fast enough for our future needs
 - Good life expectancy



Digisonde 4D Transceiver Layout: Current System

LPT for control of hardware in card cage
IDE DMA delivery of receiver data
RTEMS hardware support limits computer options

TRANSCEIVER (UPPER) CHASSIS



Digisonde 4D Layout: Fully Implemented Transceiver

All transceiver functionality implemented as a single transceiver PCIe card
Replace RTEMS with RTLinux
Integrate function of Control and Data computer into a single platform

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Benefits

- Single interface to computer means any computer with a PCIe bus is a candidate for our system
- Replacing ASIC components with firmware implemented on FPGA provides us greater development control
- All our technology on one device (ideally)
- Good platform to expand functionality of the Digisonde
- More flexible to keep up with technology as it evolves





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Tracker Filter



Digital Receiver



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Preprocessor Card



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BIT-Card





Power Distribution Card





S/N 16

POWER DISTRIBUTION REV WELL CENTER FOR ATM

Digisonde 4D Transceiver Layout: Pre-Processor as PCIe Card

Move Pre-Processor functionality to PCIe card on **Control Computer bus**

PROC **CONTROL CPU** LPT NETWORK XMTR RCVR TRK BIT DATA CPU TX1 ANT. SWITCH TX2 DRIVES POWER DISTRIBUTION

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Change

Initially implement Pre-Processor as PCIe card
 Minimal changes to current system

 Eventually migrate the digital transceiver into a PCIe card

